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Some Aspects of Thyristor Series Operation

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Thyristors may be connected in series, so that the operating voltage of the circuit can be greater than the maximum voltage rating of a single device. Differences between the characteristics of individual thyristors can lead to unequal voltage sharing, and to possible destruction of devices by excessive voltages during the off state or in the interval between the turn-on of one thyristor and another. The principles of protection by means of parallel capacitors, parallel resistors, and series inductors are discussed; and the lines along which the design of practical protective circuits should proceed are indicated.

INTRODUCTION

When it is not possible to obtain a thyristor (SCR) with a crest working voltage rating that is high enough for the requirements of a particular application, two or more thyristors can be connected in series. By this means the voltage that can be used is, ideally, n times the voltage rating of a single thyristor, where n is the number of thyristors in the chain.

In practice, certain precautions must be taken if a reasonably close approach to this ideal is to be achieved. There may be a considerable spread in the leakage currents of individual thyristors of any particular type; so that, in the blocking state, the applied voltage may not be equally shared between the thyristors, and the voltage drop across one of them may exceed the maximum voltage rating for the type.

A further complication is that the difference in turn-on times between individual thyristors can cause high transient voltages to appear across the slower devices during the turn-on process.

This introductory article discusses these problems and also describes how they may be overcome. With all Mullard thyristors available at the present time it is essential not to exceed the rated maximum repetitive peak forward blocking voltage, therefore in this article it is assumed that this rating shall not be exceeded.

Only a limited number of the relevant aspects of series operation are considered. The article must therefore be regarded as an approach to the problem rather than as a rigorous and comprehensive treatment. It is advisable to incorporate adequate safety factors in practical circuit design.

FORWARD AND REVERSE VOLTAGE SHARING

Fig. 1 shows two thyristors connected in series. In the non-conducting state, the voltage across each device will depend on the leakage currents, which are not necessarily equal. To cater for the spread in leakage current it is necessary to shunt each device with a resistor R to obtain voltage sharing. As the spread of leakage current may be considerable, it is convenient when estimating the value of R to assume that the series chain is composed of one thyristor with negligible leakage current and shunting resistance high and (n-1) with maximum leakage current I_{max} (at maximum junction temperature) and shunting resistance low. This would cause the maximum voltage to appear across the thyristor which has negligible leakage current. In this case it can be shown (Ref. 1) that:

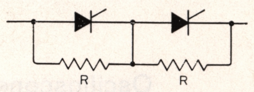


Fig. 1—Resistor sharing

$$R \leqslant \frac{1}{I_{max}}\left(\frac{V_1}{1+\beta} - \frac{v_{pk}-V_1}{(n-1)(1-\beta)}\right) \qquad \ldots(1)$$

where

V_1 = maximum voltage appearing across any thyristor, which must be $<V_R$, the crest working voltage rating of each thyristor
v_{pk} = peak voltage applied to chain
I_{max} = maximum leakage current at $T_j$max
n = number of thyristors in series
β = resistor tolerance = $\Delta R/R$

The resistors will ensure voltage sharing in both the forward and reverse direction if the forward and reverse leakage currents are less than I_{max}. When selecting R, the voltage overshoot caused by differences in the turn-on time must be considered. This is discussed on page 269.

TRANSIENT VOLTAGE SHARING

When the supply is connected to a chain of non-conducting thyristors, they will share the switch-on transient only if their anode-cathode capacitances are equal. Unfortunately, this capacitance may vary between devices, and to ensure equal capacitances it is necessary to connect capacitors in parallel with the thyristors, as shown in Fig. 2. The value of C is usually chosen to swamp the variation of the anode-cathode capacitance. Thus, for the BTY87 series, C is usually greater than 0·01μF.

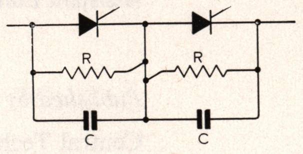


Fig. 2—Resistor and capacitor sharing

In 'back-to-back' (inverse parallel) circuits, duplication of components can be avoided by means of the arrangement shown in Fig. 3.

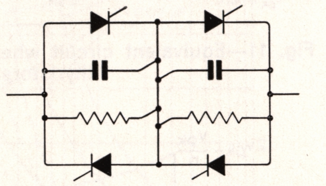


Fig. 3—Resistor and capacitor sharing in 'back-to-back' circuit

SHARING THE TURN-ON TRANSIENT

Fig. 4 shows a typical turn-on characteristic for a thyristor with a resistive load. It will be noticed that, after the application of the gate voltage, there is a delay t_d. The anode current rises very slightly during this period. The gate pulse should be steep-fronted.

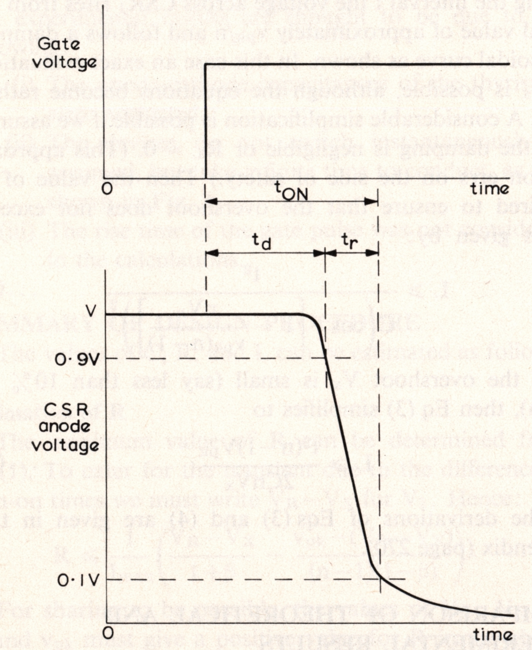


Fig. 4—Typical turn-on waveform for a resistive load

When the anode current has risen to a certain value, the thyristor is rapidly turned on. The turn-on time t_{ON} can be expressed as t_d+t_r, and t_{ON} may vary considerably between samples. It is possible to reduce t_d (and probably also the spread of t_{ON}) by overdriving the gate, but keeping within the gate current rating.

The waveforms obtained in a simple half-wave rectifier circuit, Fig. 5, when the series chain consists of a faster and a slower thyristor, are shown in Fig. 6. It will be noticed that a transient appears across the slower thyristor and may cause its voltage rating to be exceeded because C is usually too small to enforce sharing. Two methods of overcoming this problem are:

(i) To increase the value of C to enforce sharing,
(ii) To place a small inductance in series with the load, if the load itself is non-inductive.

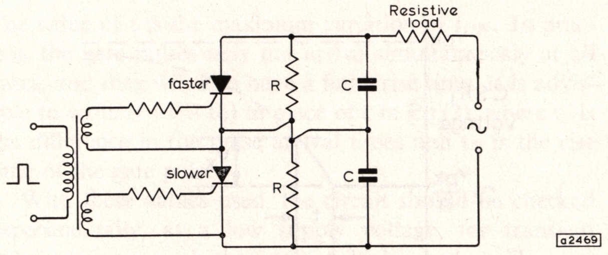


Fig. 5—Half-wave rectifier circuit. One thyristor has fast turn-on time, one slow

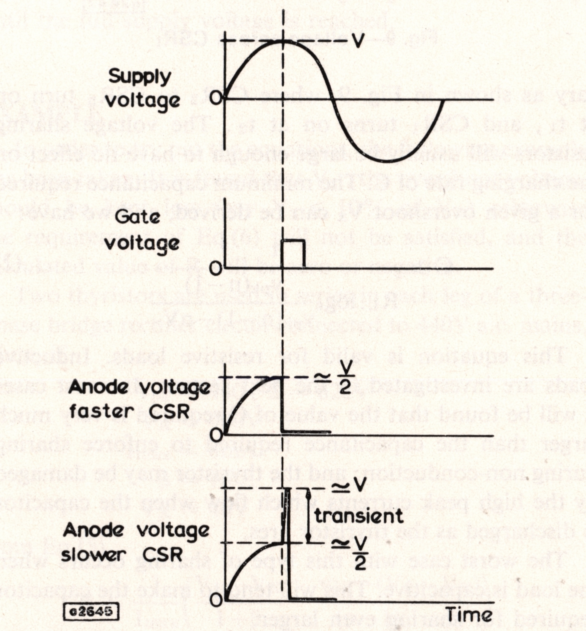


Fig. 6—Waveforms in half-wave rectifier circuit with fast and slow thyristors

Capacitor Sharing

Consider the worst case when all the thyristors except one, in the circuit of Fig. 7, turn on simultaneously, with the supply voltage at a maximum, and the slow thyristor CSR_1 fires after a delay t. This is an approximation, but it enables the value of C to be estimated if we assume that t is the maximum spread of t_{ON}.

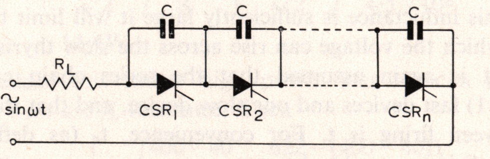


Fig. 7—Capacitor sharing

The equivalent circuit while CSR_1 is off and the others are on is shown in Fig. 8. The voltage across CSR_1 will

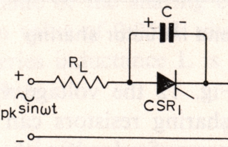


Fig. 8—Equivalent circuit when CSR_1 is off and all other thyristors are on

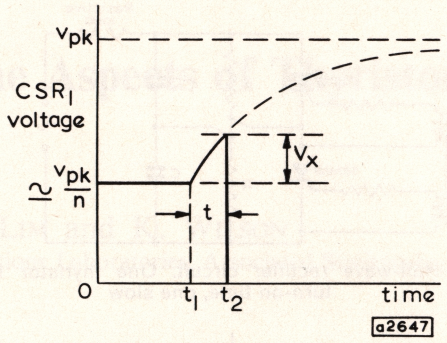


Fig. 9—Voltage across CSR$_1$

vary as shown in Fig. 9, where CSR$_2$ to CSR$_n$ turn on at t_1, and CSR$_1$ turns on at t_2. The voltage sharing resistors will usually be large enough to have no effect on the charging rate of C. The minimum capacitance required for a given overshoot V_x can be derived, and we have:

$$C \geqslant \frac{t}{R_L . \log_\varepsilon \dfrac{v_{pk}(n-1)}{v_{pk}(n-1)-nV_x}} . \qquad \ldots(2)$$

This equation is valid for resistive loads. Inductive loads are investigated in the next section. In most cases it will be found that the value of C required is very much larger than the capacitance required to enforce sharing during non-conduction; and the thyristor may be damaged by the high peak currents which flow when the capacitor is discharged as the thyristor fires.

The worst case with this type of sharing occurs when the load is capacitive. This will tend to make the capacitor required for sharing even larger.

Capacitor and Inductor Sharing

With capacitor and inductor sharing, the capacitor has the usual small value ($\simeq 0{\cdot}01\mu$F) required for equalising the anode-cathode capacitance, and an inductance is assumed in series with the thyristors. For resistive loads it may be necessary to add the extra inductance; but fortunately, in practice, most loads contain some inductance. If this inductance is sufficiently large it will limit the rate at which the voltage can rise across the slow thyristor.

It is again assumed that the series chain contains $(n-1)$ fast devices and one slow device, and that the delay between firing is t. For convenience, t_r (as defined in Fig. 4) is assumed to be zero.

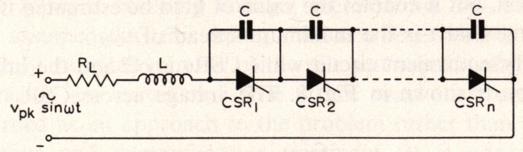


Fig. 10—Capacitor and inductor sharing

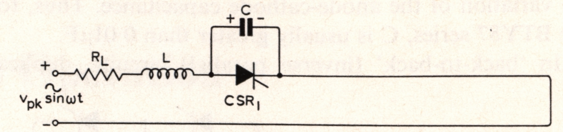


Fig. 11—Equivalent circuit when CSR$_1$ is off and all other thyristors are on

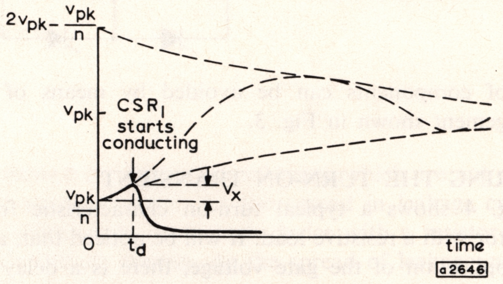


Fig. 12—Voltage across CSR$_1$

Fig. 10 shows the arrangement, and CSR$_1$ is the slow device. Fig. 11 shows the equivalent circuit after the fast thyristors have fired, and Fig. 12 the voltage variation across CSR$_1$. The voltage-sharing resistors can usually be neglected. The thyristors are fired when the supply voltage has its maximum value. It will be noticed that during the interval t the voltage across CSR$_1$ rises from its initial value of approximately v_{pk}/n and follows a damped sinusoidal curve as shown. In this case an exact evaluation of V_x is possible, although the equations become rather long. A considerable simplification is possible if we assume that the damping is negligible or $R_L = 0$. (This approximation errs on the side of safety.) Then the value of L required to ensure that the overshoot does not exceed V_x is given by:

$$L \geqslant \frac{t^2}{C\left(\cos^{-1}\left[1-\dfrac{nV_x}{v_{pk}(n-1)}\right]\right)^2} \qquad \ldots(3)$$

If the overshoot V_x is small (say less than 10% of v_{pk}/n), then Eq (3) simplifies to

$$L \geqslant \frac{t^2(n-1)V_{pk}}{2CnV_x} . \qquad \ldots(4)$$

The derivations of Eqs (3) and (4) are given in the Appendix (page 270).

COMPARISON OF THEORETICAL AND EXPERIMENTAL RESULTS

Two 200V thyristors have been tested in the circuit shown in Fig. 13. Measurement of the two devices showed that $t \simeq 1{\cdot}6\mu$s. The results of these experiments are shown in Fig. 14, with the theoretical values for comparison.

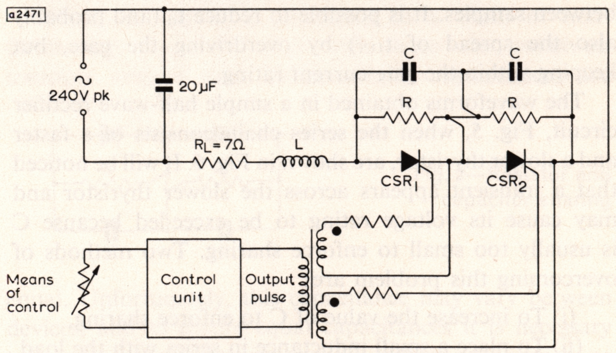


Fig. 13—Circuit for determination of degree of sharing

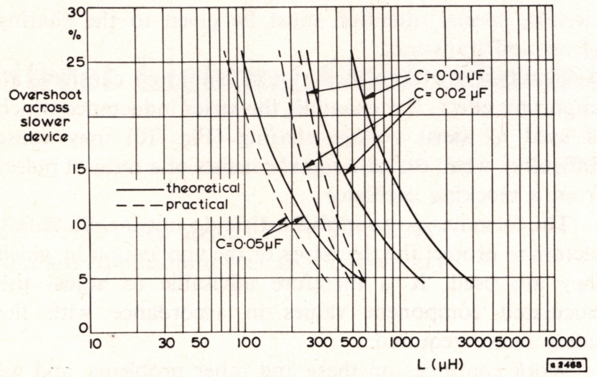


Fig. 14—Comparison of observed and theoretical results

Considering the approximations made in the calculations, the results agree reasonably well and yield 'safe' component values. The differences between the theoretical and experimental results are thought to be due to the following:

(i) The anode-cathode capacitances of the thyristors were neglected.

(ii) The devices do not switch instantaneously as assumed, but take a finite time to conduct, as was shown in Fig. 3.

(iii) The rise time of the gate pulse was not considered in the calculations.

SUMMARY OF DESIGN PROCEDURE

The values of C, R, and L can be estimated as follows:

Estimation of R

The maximum value of R can be determined from Eq (1). To cater for the transient due to the difference in turn-on times we must write $V_R - V_X$ for V_1. Hence:

$$R \leqslant \frac{1}{I_{max}}\left(\frac{V_R-V_X}{1+\beta} - \frac{v_{pk}-(V_R-V_X)}{(n-1)(1-\beta)}\right) . \qquad \ldots(5)$$

For sharing to be possible, the values of V_R, V_X, β, n, and v_{pk} must give a positive value for R in the above expression. The condition for R to be always positive is:

$$v_{pk} < \left(2-n+\frac{2(n-1)}{1+\beta}\right)(V_R-V_X) \qquad \ldots(6)$$

The minimum value of R is determined by its power dissipation. The example given on this page shows how R can be determined in a practical case.

Estimation of C

The value of C is selected to swamp variations in the anode-cathode capacitance. Usually, C lies in the range 0·01 to 0·05μF. Excessive values of C, say >0·1μF, may damage the thyristors, because a large current flows as the device is fired and C is discharged.

Estimation of L

The minimum value of L required to ensure that the turn-on transient does not exceed the value of V_x assumed in the estimation of R, can be estimated from Eq (3). The value of t is the maximum variation of t_{ON}. In practice, the gate pulses may not arrive simultaneously at all gates, and they will also have a finite rise time. It is advisable to write $(t+t_1+t_G)$ in place of t in Eq (3), where t_1 is the difference in the pulse arrival times and t_G is the rise time of the gate pulse.

With these values used, the circuit should be checked experimentally, at a low supply voltage, for transient voltages across each thyristor. A high-speed oscilloscope is required. If all is correct, the supply voltage can be increased in steps, the circuit being inspected at each step until the full supply voltage is reached.

EXAMPLE

In order to try out the equations, the following example has been taken. It is found that V_x, the overshoot voltage, should be kept low (say $V_x \leqslant 10\%$ of V_R) otherwise the requirement of Eq (6) will not be satisfied, and the calculated value of R will be zero or negative.

Two thyristors are used in series in each leg of a three-phase bridge rectifier circuit connected to 440V a.c. mains. Then, if

$$\begin{aligned} v_{pk} &= 440\sqrt{2} = 622\text{V} \\ V_R &= 400\text{V} \\ I_{max} &= 8\text{mA} \\ \beta &= 10\% \\ V_X &= 40\text{V} \end{aligned}$$

from Eq (5)

$$\begin{aligned} R &\leqslant \frac{1}{I_{max}}\left(\frac{V_R-V_X}{1+\beta} - \frac{v_{pk}-(V_R-V_X)}{(n-1)(1-\beta)}\right) \\ &\leqslant \frac{1}{8\times10^{-3}}\left(\frac{400-40}{1+0{\cdot}1} - \frac{622-(400-40)}{(2-1)(1-0{\cdot}1)}\right) \\ &\leqslant 4{\cdot}5\text{k}\Omega . \end{aligned}$$

The maximum power P dissipated in this resistor occurs when the thyristors are non-conducting. Thus

$$\begin{aligned} P &= \left(\frac{V_R-V_X}{\sqrt{2}}\right)^2 \cdot \frac{1}{R} = \left(\frac{400-40}{\sqrt{2}}\right)^2 \cdot \frac{1}{4{\cdot}5\times10^3} \\ &= 14{\cdot}4\text{W}. \end{aligned}$$

To reduce this rather high power loss we can use resistors with a 5% tolerance. Then

$$\begin{aligned} R &\leqslant \frac{1}{8\times10^{-3}}\left(\frac{400-40}{1+0{\cdot}05} - \frac{622-(400-40)}{(2-1)(1-0{\cdot}05)}\right) \\ &\leqslant 8{\cdot}6\text{k}\Omega \text{ (say } 8{\cdot}2\text{k}\Omega) \end{aligned}$$

and

$$P = \left(\frac{360}{\sqrt{2}}\right)^2 \cdot \frac{1}{8{\cdot}2\times10^3} = 7{\cdot}9\text{W} ,$$

so that 10W resistors may be used.

The value of the sharing capacitor C is taken as the maximum value of 0·05μF given on page 269.

The series inductance L is calculated as follows from Eq (3). Thus

$$L \geqslant \frac{t^2}{C\left[\cos^{-1}\left(1-\dfrac{nV_x}{v_{pk}(n-1)}\right)\right]^2} .$$

With t = 3μs,

$$L \geqslant \frac{(3\times10^{-6})^2}{0{\cdot}05\times10^{-6}\left[\cos^{-1}\left(1-\dfrac{2\times40}{622\times(2-1)}\right)\right]^2}$$

$$\geqslant 678\mu\text{H}.$$

This means that the total inductance in the load circuit must be equal to or greater than 678μH.

OTHER CONSIDERATIONS

This article has discussed only the more important questions that arise when thyristors are operated in series. When a fully-engineered circuit is to be designed, a number of other aspects must be taken into account. For example, the factors which probably caused the discrepancies between the theoretical and practical results (see page 269) should be considered; and, in addition, spreads in turn-on time and anode-cathode capacitance may have a significant effect.

In particular cases, there may be special design problems. Thus, when thyristors are used in series in inverter circuits, special attention must be given to the sharing of turn-off transients.

Finally, the type of firing pulse employed can have an important effect. For example, the series inductance which is used to assist voltage sharing (Fig. 10) may cause difficulties when the gate signal consists of a train of pulses from a blocking oscillator.

The formulas given in this article do not include safety factors to protect the thyristors or the application in which they are used. It is therefore advisable to adjust the calculated component values in accordance with the safety factor required.

Work continues on these and other problems, and we hope to discuss further aspects of series operation in a later article.

Ref. 1. Dayal, M. 'Power Rectification with Silicon Diodes'. **Mullard Technical Communications,** Vol. 7, No. 68, Jan. 1964, p. 260.

APPENDIX

Voltage Sharing Using a Series Inductor

Fig. 10 shows the circuit diagram; Fig. 11 the equivalent circuit after CSR_2 to CSR_n have fired, with CSR_1 still non-conducting; and Fig. 12 the voltage waveform across CSR_1.

In Fig. 11, after CSR_2 to CSR_n have fired, the voltage across CSR_1 is approximately v_{pk}/n. The voltage across CSR_1 will rise as the LCR circuit oscillates. As R_L is present, the oscillation will be damped as shown in Fig. 12. The voltage overshoot V_x can be calculated from this circuit, but the solution is rather long.

It is convenient to assume that $R_L = 0$ in view of the approximations already made, and the additional error introduced is on the side of safety. In this case the transient voltage appearing across C takes the form of a cosine wave of amplitude.

$$v_{pk}\left(1-\frac{1}{n}\right),$$

hence

$$v_{pk}\left(1-\frac{1}{n}\right)-V_x = v_{pk}\left(1-\frac{1}{n}\right)\cos\omega t$$

where $\omega^2 = 1/LC$.

From these equations we have:

$$L \geqslant \frac{t^2}{C\left[\cos^{-1}\left(1-\dfrac{nV_x}{v_{pk}(n-1)}\right)\right]^2}.$$

If V_x is small,

$$\cos^{-1}\left(1-\frac{nV_x}{v_{pk}(n-1)}\right)$$

is small, and we may write:

$$\cos^{-1}\left(1-\frac{nV_x}{v_{pk}(n-1)}\right) = \sqrt{\frac{2nV_x}{v_{pk}(n-1)}}$$

since $\cos\theta \simeq 1-\dfrac{\theta^2}{2}$ if θ is small.

Hence

$$L \geqslant \frac{t^2(n-1)v_{pk}}{2CnV_x}.$$

Street Lighting Controller using a Photoconductive Cell

G. F. Jeynes and G. J. Thomas
Mullard Applications Research Laboratory

A sensitive automatic controller for street lighting is described. It switches at predetermined daylight levels rather than at predetermined times, thus catering both for abnormal dark periods at dusk, dawn, or during the day, and for the special needs of (say) tree-lined streets. A delay circuit obviates erroneous switch-off by lightning flashes and other transient illumination. The unit is immune to the results of power failures; and in cost and power consumption also, it compares favourably with conventional clock controllers.

INTRODUCTION

Automatic control of artificial lighting is used in a wide range of situations; for example, factory lighting, the lighting of goods depots and marshalling yards, and conventional street lighting. Most street lighting systems utilise a synchronous clock mechanism, either for individual lamp standards or, in some cases, for groups of standards. These clocks turn the lamps on at lighting-up time and turn them off again at midnight or dawn, depending upon the policy of the local lighting authority.

Two types of synchronous clock mechanism are in general use. In the cheaper and more popular form, a synchronous motor is coupled to a solar dial, and the unit automatically makes adjustments for the seasonal variations which give rise to changes in the required switching time. In the event of a power failure, the timing mechanism will be delayed by a time equivalent to the duration of the failure. A second mechanism, which finds less general use, incorporates a spring reserve to keep the timing action correct for up to nine hours without the mains supply.

These two control techniques have a number of disadvantages in common. They cannot take account of variations in light level which may occur at about the normal switching time. For example, on an overcast evening an early switch-on would be desirable; but the mechanism adheres to the preset switch-on time, so that there is a period during which the street is inadequately lighted. Neither can they allow for low light levels in tree-lined roads.

This article describes a simple cadmium sulphide street lighting control which has the advantage of the more expensive of the clock control units in that its operation is not affected by a history of mains failures. In addition, its switching action is related to the light level actually present, rather than to time. The unit as described does not, of course, cater for switch-off at midnight or similar time-dependent programmes.

The price of the unit will probably be lower than that of the controller with the simple synchronous motor coupled with a solar dial.

GENERAL REQUIREMENTS

In a street lighting controller which operates by sensing the ambient light level, the switching levels must be related to the official lighting-up time, which, in the United Kingdom, is 30 minutes after sunset.

Fig. 1 gives a typical curve of light level with respect to time, taken at dusk. The line A–A shows the daylight level at the official lighting-up time for road vehicles on a particular evening (16 April, 1963) in Reigate, Surrey. It was observed that all the street lights were switched on at a level of >27 lux; that is, some 15 minutes earlier than lighting-up time. As it is difficult to obtain a precise sensitivity level requirement from these results, the approach has been to design the controller to be as sensitive

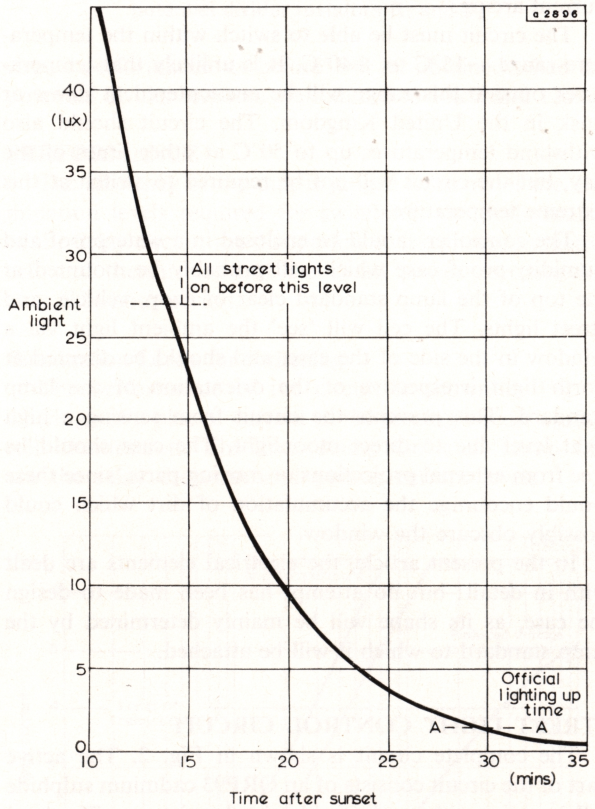


Fig. 1—Typical variation of light level with time, at dusk

as possible. This enables the user to select a less sensitive level, if necessary, by masking the light input to the unit.

A number of measurements of background light levels indicate that in a well-lit street the light level at night (excluding light from shop windows) is not greater than about half a lux. Therefore switching at a level of some 3 lux is taken as a target requirement.

The circuit has to incorporate a delay to prevent the street light being switched off during the night by spurious flashes of light. This is essential where mercury or sodium vapour lamps are used, since 10 to 15 minutes have to elapse while the lamp cools down sufficiently to restrike.

A delay of 2 seconds is adequate protection against brief, intense flashes such as lightning, while approximately 10 seconds is satisfactory for low-level flashes of longer duration. However, to avoid difficulties in setting up the unit, the delay should not exceed 30 seconds.

The circuit should operate from any mains supply voltage encountered in the United Kingdom (200V to 250V r.m.s.) without adjustment to the electrical circuit. In addition, the circuit must tolerate supply voltage variations of +10% to −15% about any given value.

The switching response at the required level has to be positive, and a built-in backlash or difference between switching on and switching off enhances the positive action. Snap action switch contacts are desirable to avoid load current arcing.

The circuit must be able to switch within the temperature range −15°C to +40°C. It is unlikely that temperatures outside this range will be encountered at dawn or dusk in the United Kingdom. The circuit should also withstand temperatures up to 50°C at other times of the day, but the circuit will not be required to switch at this extreme temperature.

The controller should be enclosed in a waterproof and humidity-proof case which will probably be mounted at the top of the lamp standard clear of shop, vehicle, and street lights. The cell will 'see' the ambient light via a window in the side of the case, and should be directed at north light irrespective of the orientation of the lamp standard. This prevents the circuit from sensing a high light level due to direct moonlight. The case should be free from external projections or moving parts, since these would encourage the accumulation of dirt which could possibly obscure the window.

In the present article, the electrical elements are dealt with in detail; but no attempt has been made to design the case, as its shape will be mainly determined by the lamp standard to which it will be attached.

STREET LIGHT CONTROL CIRCUIT

The complete circuit is shown in Fig. 2. The active part of the circuit consists of an ORP93 cadmium sulphide cell in series with a relay and a load resistance. The load resistance is a Varite thermistor (negative temperature coefficient resistor) which acts as the delay element in the circuit.

The relay used in experimental models is a normal series 3000 P.O. type. The yoke actuates the plunger of a Bulgin S503 microswitch, in place of the standard contacts. This microswitch is chosen because of the low operating force required for switching a load of 5A at 250V. It should be noted that this particular combination is taken simply for convenience, and less expensive combinations are probably available.

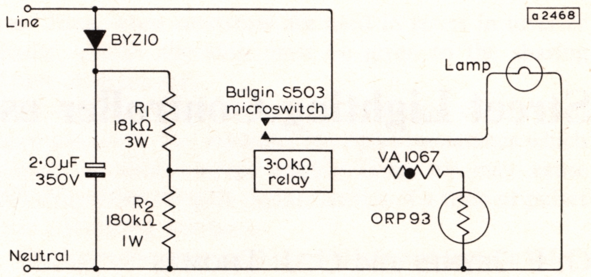


Fig. 2—Complete street light control circuit using ORP93

When the cell is illuminated at a very low light level, the current through the thermistor, relay, and cell is low, so that the dissipation in the thermistor is small and the component has a high resistance. If the cadmium sulphide cell is then illuminated at a high light level, the cell resistance falls and the current rises; but the current is limited by the high resistance of the thermistor, so that the relay cannot close. The resistance of the thermistor then falls as the dissipation rises, until after a certain delay the relay pulls in. This delay is of the order of several seconds, depending on the intensity of the illumination and also on the background light level. A brief illumination, even at a high light level, will not produce sufficient heating of the thermistor to reduce its resistance to the value at which actuation of the relay will take place.

The remainder of the circuit (diode, capacitor, and potential divider network) provides a d.c. supply voltage.

Circuit Design

The ORP93 cadmium sulphide cell is chosen, since it has a maximum power dissipation rating of 1·0W at 25°C, and a maximum supply voltage rating of 275V r.m.s. on 400V d.c. The operating conditions in the circuit are within these ratings. The illumination/resistance characteristic of the ORP93 is given in Fig. 3. For design purposes a maximum resistance cell, as shown by line B–B, is considered, since any more sensitive cell may be induced to behave as a maximum resistance cell by placing a shutter partly across the window of the completed unit. The end-of-life condition shown by line C–C is taken as a 50% increase in cell resistance over life for a given illumination.

The choice of relay coil resistance is a compromise between conflicting requirements. For high sensitivity, a high resistance coil is necessary; however, there is a limit to the sensitivity desired. The most sensitive switch-on condition (when the relay drops out) should be at a current which is sensibly higher than the current expected when the circuit operates under the ambient light level at night.

Conversely, to achieve a satisfactory delay the resistance of the relay plus the output impedance of the potential divider must be much lower than the 'cold' resistance of the thermistor.

With a thermistor type VA1067, which has the highest nominal value currently available (excluding low-dissipation types), the desired circuit performance is given by a total series resistance of about 20kΩ, used in conjunction with relay operating currents of pull-in ≤4mA and drop-out ≥0·75mA.

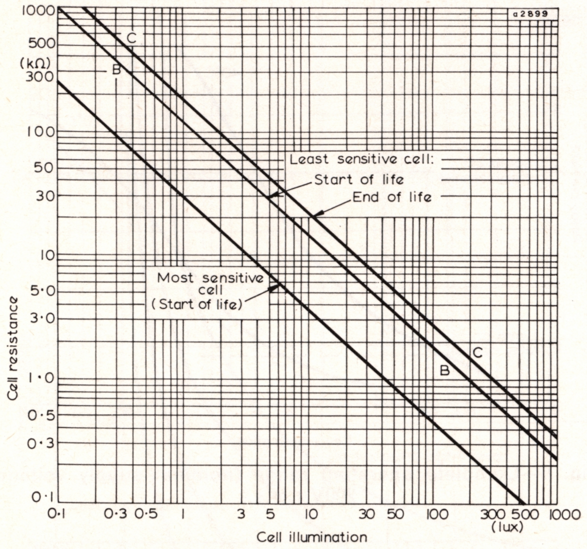


Fig. 3—ORP93: variation of cell resistance with illumination

The total circuit resistance of 20kΩ plus the value of the thermistor is also sufficient to keep the power dissipated in the cadmium sulphide cell within the 1W rating under all operating conditions.

Finally, the impedance of the potential divider limits the mean d.c. voltage across the smoothing capacitor to less than 350V. This 2μF capacitor is connected directly to the rectifier and not to the centre tap of the potential divider, in order to keep the charging impedance low and thus to obtain a high rectifying efficiency.

With this circuit configuration a diode with a peak inverse voltage rating of at least 740V and a forward current rating of at least 15mA is required. The BYZ10 is a suitable type.

Relay Coil Resistance

Although it is necessary to keep the total of the relay resistance and the potential divider output resistance constant at about 20kΩ in this design, a range of relay and potential divider resistors may be selected to satisfy this condition. Fig. 4 shows the required relationship between the potential divider resistors (shown as R_1 and R_2 in Fig. 2) as a function of the relay coil resistance, assuming the relay pull-in current is ≤4mA and the drop-out current is ≥0·75mA. With this curve the relay and potential divider resistances can be selected to satisfy particular equipment requirements.

For example, a conventional P.O. series 3000 relay with a coil resistance of 3·0kΩ is used with 18kΩ and 180kΩ potential divider resistors, as shown in Fig. 2. However, a less expensive solution can probably be obtained by using a relay of cheaper and therefore less sensitive construction with, say, a 10kΩ coil resistance, but with pull-in and drop-out currents remaining at ≤4mA and ≥0·75mA. Under these conditions the same circuit performance as before will be obtained when the potential divider resistors are reduced to 10kΩ and 120kΩ.

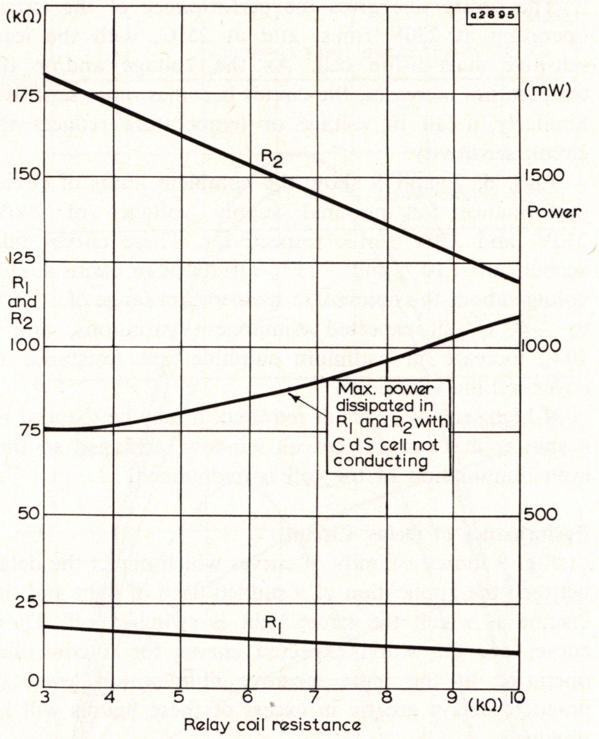


Fig. 4—Relationship between relay coil resistance and potential divider resistors R_1 and R_2

PERFORMANCE

The efficiency of the unit is judged in terms of the illumination levels required for switching, the performance of the delay circuit, the dissipation in the photoconductive cell and thermistor, and the mean power consumption over a 24-hour period.

Illumination Levels for Switching

The performance of the circuit is shown in Fig. 5, which gives a plot of current in the sensing circuit against cell illumination. The lines 'Lamp On' and 'Lamp Off' are the relay drop-out and pull-in current levels.

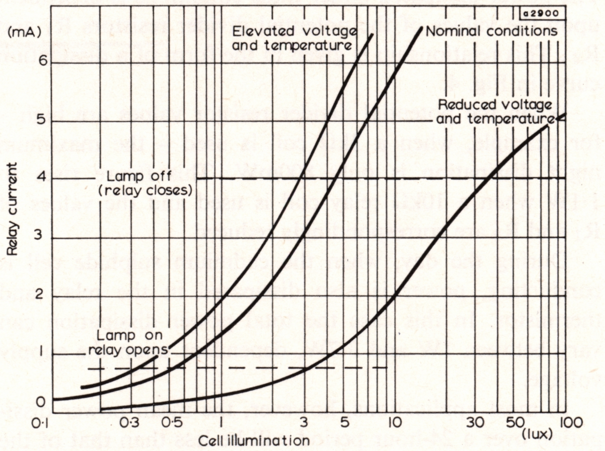


Fig. 5—Performance characteristics

The centre line gives the performance of the circuit operating at 230V r.m.s. and at 25°C, with the least sensitive start-of-life cell. As the voltage and/or the temperature increases, the circuit becomes more sensitive. Similarly, a fall in voltage or temperature reduces the circuit sensitivity.

Figs. 6, 7, and 8 show the complete limits of circuit performance for nominal supply voltages of 200V, 230V, and 250V r.m.s. respectively. These curves take account of +10% and −15% variations in mains supply voltage about the nominal, a temperature range of −15°C to +40°C, all expected component variations, and a 50% increase in cadmium sulphide cell resistance to cover cell life variations.

If high sensitivity is not required, it may be reduced by a shutter in front of the cell window, arranged so that even illumination of the cell is maintained.

Performance of Delay Circuit

Fig. 9 shows a family of curves which depict the delay between the application of a sudden flash of light and the instant at which the street light is switched off. These curves are the worst expected curves for a controller operating at the most sensitive illumination level. In practice, delays greatly in excess of these figures will be obtained.

Dissipation in Cadmium Sulphide Cell and Thermistor

A primary aim of the present design has been to obtain long life reliability by keeping the maximum dissipation in both the cadmium sulphide cell and the thermistor low. Fig. 10 gives the maximum power dissipation curves for both devices under various operating conditions. In all cases the thermistor operates well within its maximum rating of 600mW; and in all conditions except that of 275V a.c. mains supply with a temperature of 40°C, the ORP93 is within its continuous dissipation rating. In this latter case the additional dissipation should not have a significant effect on life performance, as this temperature is unlikely to occur at dusk in the United Kingdom.

Power Consumption

The total power consumption of the circuit is low during the night, the relay circuit taking little current. The power dissipated under these conditions is dependent upon the values of the potential divider resistors R_1 and R_2. This relationship is given in the form of a dissipation curve in Fig. 4.

When the potential divider resistor values are high – for example, when a 3kΩ coil is used – the maximum night dissipation is only 800mW. This figure rises to 1·1W when a 10kΩ relay coil is used and the values of R_1 and R_2 are correspondingly reduced.

During the day, when the cadmium sulphide cell is conducting, power is also dissipated in the relay and thermistor. In this case the total power dissipation can vary between 1W and 3·7W, dependent upon the supply voltage.

In most applications, however, the mean power dissipation over a 24-hour period will be less than that of the present synchronous clock timing mechanisms.

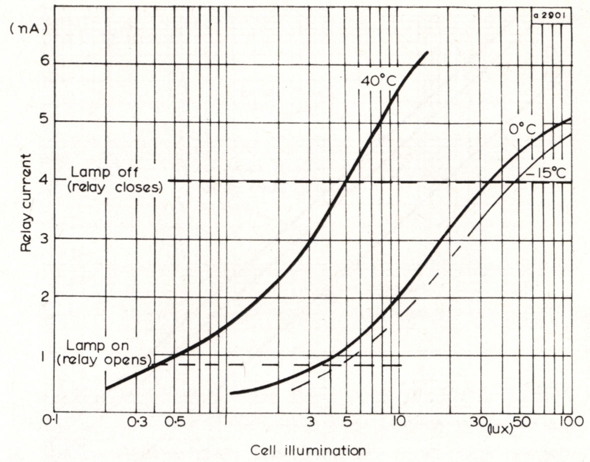


Fig. 6—Complete operating range (nominal supply voltage 200V r.m.s.)

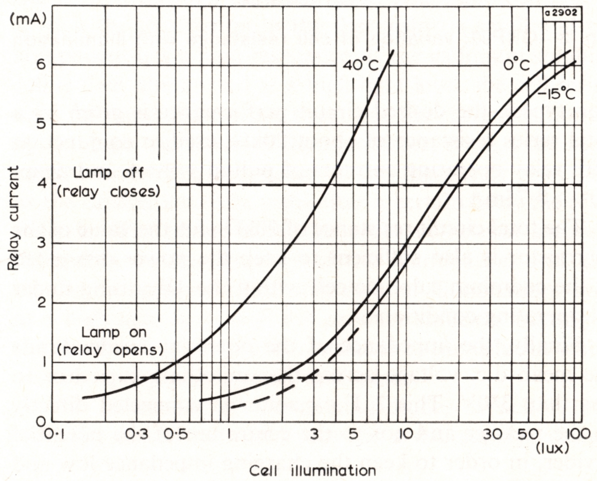


Fig. 7—Complete operating range (nominal supply voltage 230V r.m.s.)

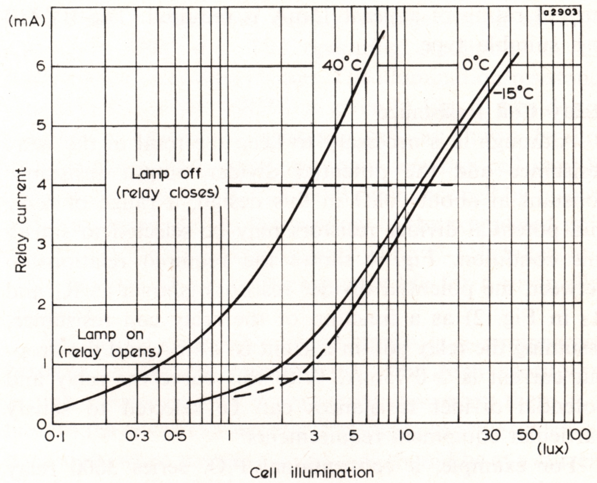


Fig. 8—Complete operating range (nominal supply voltage 250V r.m.s.)

SETTING-UP PROCEDURE

A simple shutter can provide a method of setting the controller, either during production or after the unit is installed, to switch the lights on at a predetermined light level. This method has the advantage that the ratio of ON and OFF switching levels remains constant, irrespective of the setting desired.

To set the unit up it should be connected to a supply of the same nominal value as that on the installation site. With the temperature at about 25°C the shutter can then be slowly closed until the lamps switch on at the ambient light level applied to the unit. The switch-off level is automatically set by the circuit backlash to be a few lux higher than the switch-on level. An increase in voltage of 10% and an increase in temperature to 40°C will cause the unit to switch at approximately half the setting-up illumination. Similarly, a decrease of 15% in voltage and a fall in temperature to −15°C results in the circuit switching at a level some three times higher than the setting-up level.

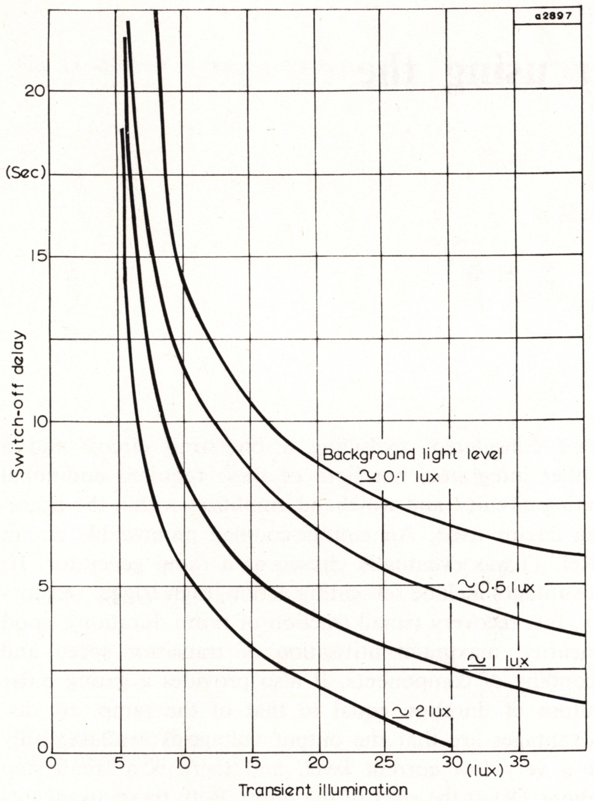


Fig. 9—Switch-off delay as a function of illumination for various background illumination levels

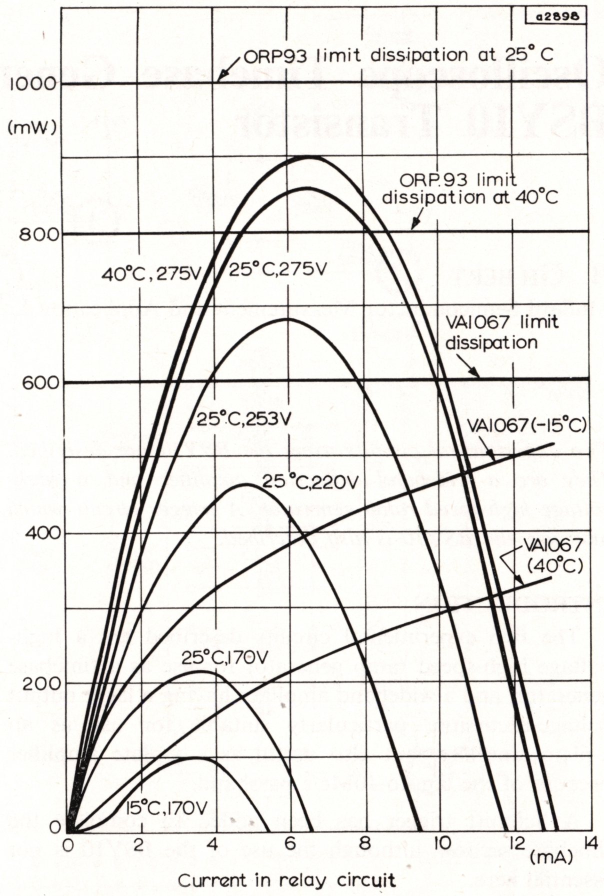


Fig. 10—Variation of dissipation in thermistor and cadmium sulphide cell as a function of relay current, at given ambient temperatures

Oscilloscope Timebase Generator using the BSY10 Transistor

B. Gilbert
Mullard Semiconductor Measurement and Application Laboratory

Two experimental circuits using the BSY10 are described. They are a wideband deflection amplifier and a high-voltage high-speed ramp generator. A trigger circuit which may use the BSY10 is also described.

INTRODUCTION

The two experimental circuits described are a high-voltage high-speed ramp generator for use as a timebase generator, and a wideband amplifier having a large output voltage-excursion, particularly suitable for use as an x-plate amplifier, but also useful as a y-plate amplifier because of the d.c.-to-10Mc/s passband.

A Schmitt trigger has been added to complete the timebase section, although the use of the BSY10 is not essential here.

The following are parameters of the BSY10, a transistor which is particularly useful for the circuits described.

Absolute Maximum Ratings	
V_{CBO} max.	+60V
I_C max.	50mA
V_{EB} max. (I_t = 0mA)	+5V
P_{tot} max. (T_{amb} = 50°C)	250mW
Characteristics	
I_{CBO} max. (T_{amb} = 25°C)	2µA
f_1 min.	60Mc/s
h_{FE} (I_E = 10mA)	45 to 80

In addition, the value of c_{obs}(at $V_{CB} = +2V$) is taken as 2pF.

No careful theoretical study of the circuits is given. Full component spreads have not been taken into account, so that some variation in performance from that quoted below may be expected. However, worst-case values for the semiconductor devices are used in the calculations.

RAMP GENERATOR

Initially it was decided to obtain the maximum amplitude possible with the BSY10, that is, about 50V. The fastest sweep speed required was about 100ns/cm when used as an oscilloscope timebase generator; the slowest sweep was clearly to be limited by capacitor size, since, to maintain accuracy of timing, the charging current must be about 100 times the maximum possible variation of leakage current. Other considerations were economy of components and good linearity. Several types of ramp generator were considered, including a bootstrap circuit and a Miller integrator, but both of these required additional gating circuits, and wideband amplifiers within the charging circuit itself. An emitter-coupled monostable circuit (Ref. 1) was eventually chosen as a ramp generator. Its advantages include self-gating action, high trigger sensitivity, fast recovery (small fraction of ramp duration), good linearity, maximum utilisation of transistor speed and economy of components. It also provides a gating pulse output of duration equal to that of the ramp. Its disadvantages are that the output voltage is available only at a very low current level, and there is a small step (about 1V) at the start of the ramp. Both these disadvantages are easily overcome.

The complete circuit is shown in Fig. 1a, but the operation is more easily explained by means of the skeleton circuit shown in Fig. 1b, which omits the emitter-follower, Tr_{102}, the trigger hold-off circuit involving D_{101}, and the constant current system involving Tr_{104}. The circuit of Fig. 1b differs from that described in Ref. 1 inasmuch as the collector voltage of Tr_1 is caught by D_3 at a potential E_2. This produces a constant ramp amplitude, irrespective of the charging current I.

Basic Operation

Consider first the stable state. When Tr_3 is conducting, its emitter current is I, and its collector voltage is at a low value, but sufficient to prevent bottoming. Tr_1 is non-conducting, since the base and emitter voltages are equal. The steady-state collector voltage of Tr_1 is

$$V_{C(1)}(0-) = E_1 - [I_{CO(1)} + I_{CO(3)} - I_{DO(3)} - (1-\bar{\alpha}_3)I]R_3 \qquad \ldots(1)$$

where

$I_{CO(1)}$ = collector leakage of Tr_1
$I_{CO(3)}$ = collector leakage of Tr_3
$I_{DO(3)}$ = reverse leakage of D_3
$\bar{\alpha}_3$ = large-signal d.c. alpha of Tr_3

The emitter voltage of Tr_3 therefore rests at

$$V_{E(3)}(0-) = V_{C(1)}(0-) - V_{BE(3)} \qquad \ldots(2)$$

where

$V_{BE(3)}$ = base-emitter voltage of Tr_3 at emitter current I.

A positive trigger pulse at the base of Tr_1 causes it to conduct slightly, and the loop comprising Tr_1, Tr_3 and C_2 becomes regenerative. This switch-on phase lasts about 20ns (in the particular case being considered), ending with the collector voltage of Tr_1 at

$$V_{C1}(0+) = E_2 - V_{D(3)} \qquad \ldots(3)$$

where

$V_{D(3)}$ = forward voltage D_3 at a current $I_{D(3)}$,

and

$$I_{D(3)} = \bar{\alpha}_1 I + I_{CO(1)} - I_{CO(3)} - I_{EO(3)} - I_{R(3)} \qquad \ldots(4)$$

where

$\bar{\alpha}_1$ = large-signal d.c. alpha of Tr_1
$I_{EO(3)}$ = emitter leakage current of Tr_3
$I_{R(3)}$ = current in R_3

$$= \frac{E_1 - V_{C(1)}(0+)}{R_3}. \qquad \ldots(5)$$

R_3 must be made large enough for the collector to catch at voltage E_2 with the smallest value of I, and yet small enough for the value of $V_{C(1)}(0-)$ to be nearly equal to E_1.

We now have constant current flowing via C_2 into the emitter of Tr_1, so that C_2 charges linearly. This action can be described by the equation

$$V_{E(3)}(0+) = V_{E(3)}(0-) - \Delta V_{E(1)} - \frac{I_{CAP}}{C_2}.t \qquad \ldots(6)$$

where

$\Delta V_{E(1)}$ = amplitude of step at emitter of Tr_1 which appeared when Tr_1 switched on.

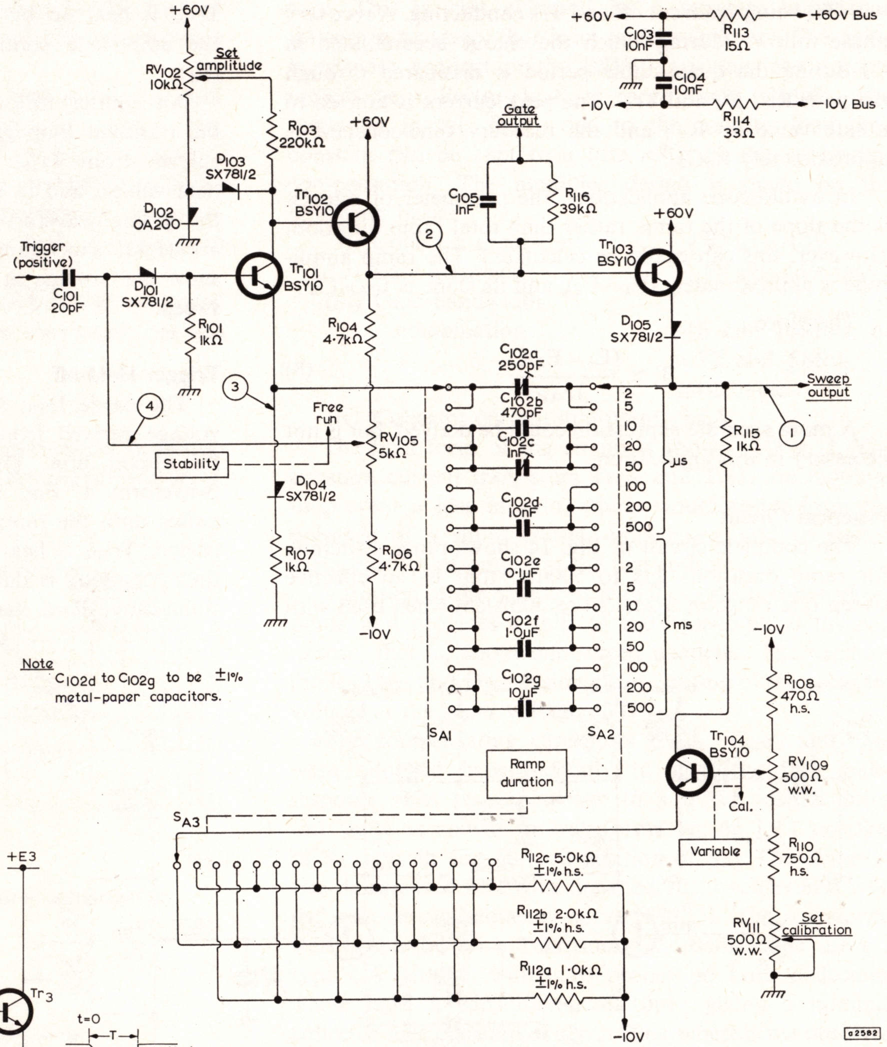
and

$$I_{CAP} = \text{capacitor current} = I + I_{EO(3)} \qquad \ldots(7)$$

The slope of $V_{E3}(0+)$ is simply I_{CAP}/C_2 volts per second, and therefore the only transistor parameter affecting slope is the emitter leakage of Tr_3. With an additional diode in the emitter this can be reduced to a negligible value.

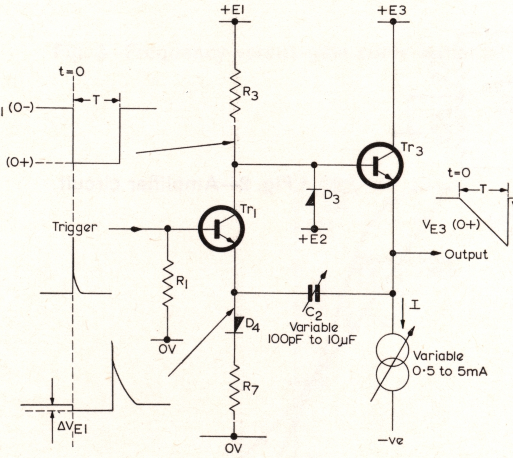
During this quasi-stable period, the loop is broken by the reverse-biased Tr_3. When C_2 has charged sufficiently negatively, Tr_3 begins to conduct and the loop becomes regenerative again. The switch-off phase ends

Fig. 1a—Circuit of ramp generator


+60V
RV102 10kΩ
Set amplitude
R103 220kΩ
D103 SX781/2
D102 OA200
+60V
Tr102 BSY10
Trigger (positive)
C101 20pF
D101 SX781/2
R101 1kΩ
Tr101 BSY10
R104 4·7kΩ
2
3
4
Free run
Stability
RV105 5kΩ
D104 SX781/2
R107 1kΩ
R106 4·7kΩ
−10V
+60V
C103 10nF
C104 10nF
R113 15Ω
+60V Bus
−10V
R114 33Ω
−10V Bus
Gate output
C105 1nF
R116 39kΩ
+60V
Tr103 BSY10
D105 SX781/2
C102a 250pF
C102b 470pF
C102c 1nF
C102d 10nF
C102e 0·1µF
C102f 1·0µF
C102g 10µF
2 5 10 20 50 100 200 500 µs
1 2 5 10 20 50 100 200 500 ms
Sweep output
1
R115 1kΩ
SA1
SA2
Ramp duration
SA3
Tr104 BSY10
−10V
R108 470Ω h.s.
RV109 500Ω w.w.
Cal.
Variable
R110 750Ω h.s.
RV111 500Ω w.w.
Set calibration
R112c 5·0kΩ ±1% h.s.
R112b 2·0kΩ ±1% h.s.
R112a 1·0kΩ ±1% h.s.
−10V
a2582

Note
C102d to C102g to be ±1% metal-paper capacitors.

Fig. 1b—Basic form of ramp generator circuit


+E1
+E3
t=0
T
VC1 (0−)
VC1 (0+)
R3
Tr3
D3
Tr1
+E2
Trigger
R1
0V
D4
C2
Variable 100pF to 10µF
I
Variable 0·5 to 5mA
R7
0V
−ve
ΔVE1
t=0
T
VE3 (0−)
VE3 (0+)
Output

with Tr_1 being again cut off and Tr_3 conducting. A recovery phase follows, during which the charge accumulated in C_2 during the quasi-stable period is dissipated through the path R_7, D_4 and Tr_3. The peak current is limited to a safe value by R_7, and the recovery time-constant is approximately R_7C_2.

In oscilloscope applications, the parameter of interest is the slope of the ramp, rather than total ramp duration. However, this can easily be calculated. The ramp amplitude is approximately (E_1-E_2), and its slope is I_{CAP}/C_2.

Therefore

$$T \simeq \frac{(E_1-E_2)C_2}{I_{CAP}}. \qquad \ldots(8)$$

A more accurate expression could be derived, but is not necessary in this application.

Practical Circuit

The complete circuit of Fig. 1a shows range switching for ramp durations 2µs to 500ms; that is, an effective sweep rate range of 0·2µs/cm to 50ms/cm when used with the appropriate deflection system. The amplifier described below extends this to 0·1µs/cm by means of an 'X2 MAGNIFIER' facility. Range interpolation is by means of R_{112}, in a 1:2:5 sequence, and a 'VARIABLE' facility (RV_{109}) permits continuous variation of the charging current over a range of 1 to 2·5. The charging current can have values down to 0·4mA, so that R_{103} must be at least 60/0·4 or 150kΩ. A value of 220kΩ is chosen to ensure that D_{103} always catches, thus maintaining a constant ramp amplitude. The catching potential (E_2) is provided by the voltage across D_{102} since it needs to be only large enough to prevent Tr_1 from bottoming. D_{102} is held on by the current of 6mA through R_{102}, the amplitude control, which varies the starting level (E_1).

An emitter follower, Tr_2, is introduced to increase the transient loop gain, to buffer the variation of base current from Tr_{103} with varying emitter currents and beta values, and to provide a loadable output point for the gating waveform. R_{116} protects the circuit against accidental short-circuiting. Waveforms 1 to 3 (Fig. 9) show the voltage at the numbered points, for the 1ms sweep.

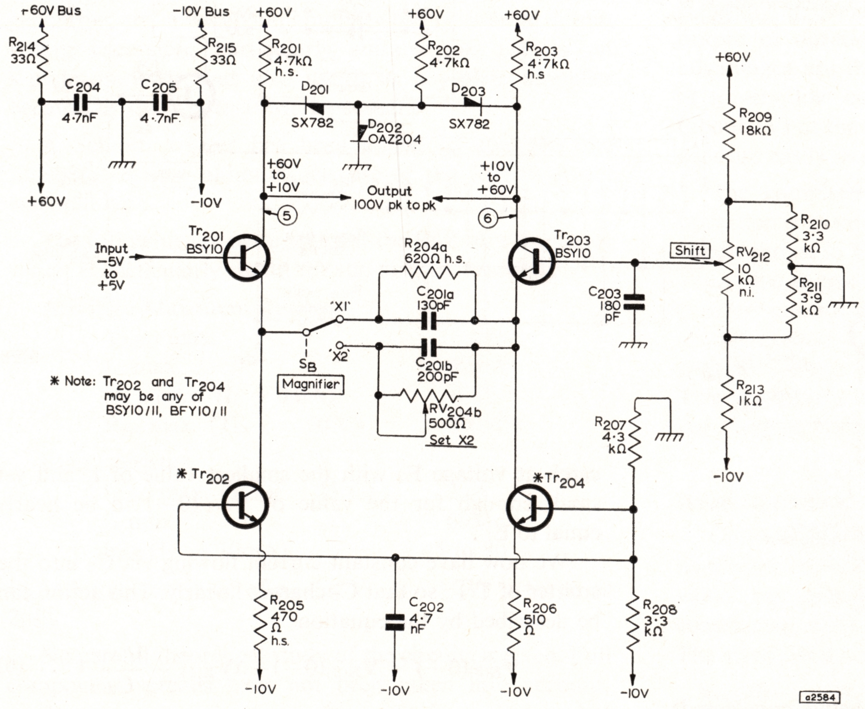


Fig. 2—Amplifier circuit

Trigger Hold-off

The diode D_{101} is nominally held at zero bias by a voltage derived from the emitter load of Tr_{102}. When the circuit fires, D_{101} is reverse-biased by about 8V (waveform 4, Fig. 9), thus holding-off further trigger pulses until the ramp is completed. During the recovery period, Tr_{101} is heavily reverse-biased (waveform 3) and thus triggering is delayed until the circuit has recovered sufficiently. R_{105} varies the degree of reverse bias on D_{101}, and hence acts as a stability control. Beyond a critical point, D_{101} is forward-biased after each recovery phase and the circuit is self-triggering.

It is important that the trigger hold-off circuit be efficient for two reasons:

(i) any trigger breakthrough on to the ramp causes velocity-modulation of the sweep. This effect is particularly likely to happen at very high trigger (sync.) rates. Tests show less than 100mV pk-to-pk breakthrough on to the 40V ramp at 10Mc/s. More careful layout, screening and decoupling would probably reduce this.

(ii) an inverted trigger pulse applied to the base of Tr_{101} during the sweep might be able to terminate the sweep prematurely.

Ideally, the hold-off system should prevent trigger pulses reaching Tr_{101} during the recovery period also, but this would require extra circuitry which is not justified. As waveforms 5j and 5k show (Fig. 9) operation under 'count-down' conditions is quite satisfactory: 5j shows the 1ms ramp triggered at 200kc/s, and 5k the 2µs ramp triggered at 10Mc/s.

The overall trigger stability at 10Mc/s was measured on the 50µs sweep and it was found that there was less than 2ns of jitter.

AMPLIFIER

In a typical case, about 70V of symmetrical deflection voltage is required for a 10cm scan. Allowing for overdrive, an output of 100V is desirable. The maximum theoretical output obtainable from two BSY10 transistors in push-pull is 120V. This amplifier design is aimed at achieving an output as near as possible to the theoretical limit, consistent with simplicity. High gain is not required, since 40 to 50V of ramp are already available from the ramp generator. However, the generator will tolerate little current loading, so that a high input impedance is necessary. This is best achieved by a separate impedance transforming stage, that is an emitter-follower. The gain-bandwidth product of the BSY10 working into a zero-impedance collector load is more than 60Mc/s. The reduction in this figure due to the collector-load time constant can be kept to a low value by use of emitter compensation. The amplifier design is made on the following basis:

(i) Collector excursion: +60 to +10V
(ii) Base excursion: ±5V absolute max.
(iii) Gain-bandwidth combination: ×6 and 10Mc/s, or ×12 and 5Mc/s, switchable
(iv) Collector current mid-point: 5mA

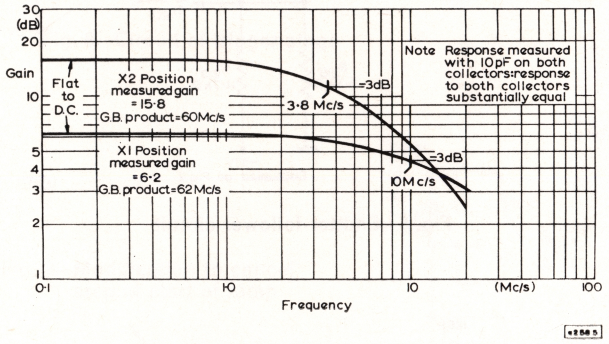


Fig. 3—Frequency-versus-gain curve for amplifier

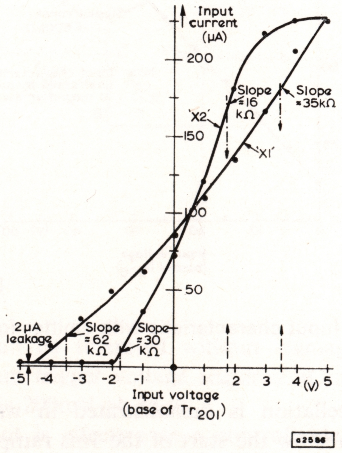


Fig. 4—Input characteristic of amplifier

The final form of the circuit is shown in Fig. 2. The constant current transistors Tr_{202} and Tr_{204} are required to prevent a loss in gain, which would result from the presence of a shunt emitter impedance, and to ensure exact balance of output at the two collectors.

Variation of the base voltage of Tr_{203} shifts the working point, and provides a shift of 100V pk-to-pk at the collectors, that is, about one screen diameter. The catching diodes D_{201} and D_{203} ensure clean limiting of the collector voltage at the zener voltage of D_{202}.

The compensating capacitors C_{201a}, C_{201b} and C_{203} were adjusted experimentally to give the best pulse response. The pulse response to a 0·5µs positive-going test pulse is shown in waveforms 5g, 6g (×1 position of S_A) and 5h and 6h (×2 position of S_A). The observed rise-times agree well with the theoretical values and with the gain-versus-frequency curve (Fig. 3). The waveforms were displayed on a Tektronix 545 oscilloscope using a type CA plug-in, with ×10 probes on both collectors. These have a capacitance of 10pF, giving a nominal collector time constant of about 50ns, whereas the observed rise-time is about 30ns. This illustrates the effectiveness of the emitter compensation. Unfortunately, compensation is only exact near the quiescent point, but is adequate for present purposes. The output terminals can be short-circuited mutually or to ground with safety.

Input Characteristic

Fig. 4 shows the input characteristic of the amplifier. It is seen that the incremental input resistance varies from 35kΩ to 62kΩ on the '×1' position, and from 16kΩ to 30kΩ on the '×2' position. For linear operation, the driving source resistance must be low. It can be simply shown that for 1% non-linearity to be introduced, this resistance must be 800Ω in the '×1' position and 340Ω in the '×2' position.

Incremental input impedance at $V_{in} = 0V$ was measured by the method of equalisation of source impedance as 40kΩ in parallel with 20pF in the '×1' position, and 25kΩ in parallel with 35pF in the '×2' position.

Emitter-follower

An emitter-follower is necessary when using the amplifier with the ramp generator, because of the high output impedance of the generator, and because of the low-impedance drive requirement of the amplifier for low distortion. The output impedance of the emitter-follower should be ideally less than 340Ω; its required input impedance can be calculated as follows. The timing capacitor in the ramp generator should ideally be driven from a constant current source for perfect linearity. Any shunt resistance appearing across the current source converts the source to a voltage source with a finite internal resistance. Thus, the capacitor charging-curve is exponentially asymptotic to this voltage, and for less than 1% distortion a target voltage of at least eight ramp amplitudes is required, that is, 400V for a 50V ramp. The smallest charging current used in the circuit of Fig. 1 is 0·4mA. Thus, the shunt resistance should be greater than 400V/0·4mA, or 1MΩ. This leads to a resistance-ratio requirement of 3000:1, which is not easily achieved. The task is eased slightly by the fact that an attenuation of about 4 to 5 times can be tolerated, since the amplifier requires only 7V pk-to-pk for 100V output.

The circuit shown in Fig. 5 is a compromise, giving a theoretical input resistance of about 500kΩ. The resistor R_{219} shifts the output by about 4V to satisfy the input requirements of the amplifier and C_{206} provides high-frequency compensation. The input characteristic of the emitter-follower is given in Fig. 6, and it shows that the actual input slope is close to the theoretical figure.

Step Cancellation

The step at the start of the ramp can be eliminated by connecting the base of Tr_{203} to the emitter of Tr_{101} via an attenuator equal in ratio to that of the emitter-follower circuit. In other words, the effective amplifier input is a fraction of the voltage appearing across the timing capacitor, and this voltage is stepless.

The modification to achieve this is shown in Fig. 7. The base decoupler, C_{203}, is removed, and it may be necessary, although the necessity did not arise in the experimental circuit, to add a high-frequency compensator, C, of a few pF. The value of R_{220} may also need some adjustment for optimum cancellation.

The voltage at point 'A' should be within ±0·1V of zero to prevent a bias voltage appearing on the emitter of Tr_{101}. This would interfere with trigger stability. R_{210} or R_{211} may therefore need slight adjustment.

Overall performance of Ramp Generator Plus Amplifier

The performance is indicated by the waveforms in Fig. 9. Waveforms 5a and 6a show the collector voltages of Tr_{201} and Tr_{203} for the 2ms ramp with the 'SHIFT' control centred. The curves show that a full 50V swing is obtainable from each collector. Waveforms 5b, 6b and 5c, 6c show the output at the extremes of the shift range: over 100V of shift (pk-to-pk) is available.

Waveforms 5d and 6d show the magnified ramp with S_{201} in the '×2' position. It is possible to obtain up to five diameters magnification but for two reasons this provision is not incorporated. Firstly, the bandwidth of the amplifier would necessarily fall to about 2Mc/s which would probably be inadequate for the faster sweeps, and secondly the gain would then be far more dependent on the transistors, because of variations in r_e. Furthermore, linearity would suffer because of the non-linear nature of r_e.

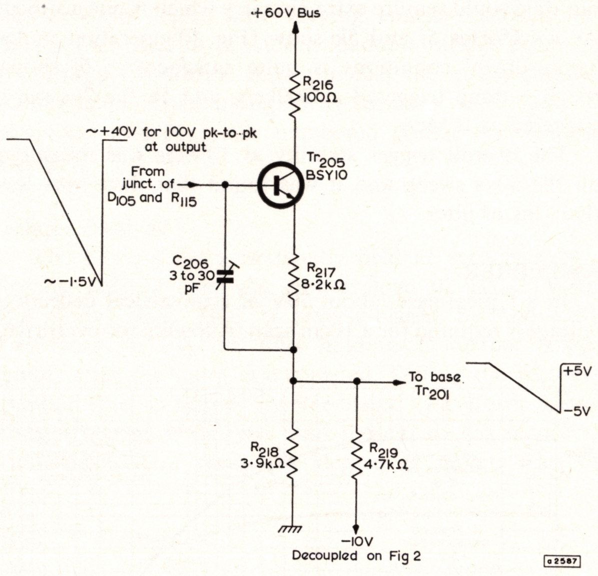

+60V Bus
R216
100Ω
~+40V for 100V pk-to-pk
at output
Tr205
BSY10
From
junct. of
D105 and R115
~−1·5V
C206
3 to 30
pF
R217
8·2kΩ
To base
Tr201
+5V
−5V
R218
3·9kΩ
R219
4·7kΩ
−10V
Decoupled on Fig 2
a2587

Fig. 5—Emitter-follower circuit

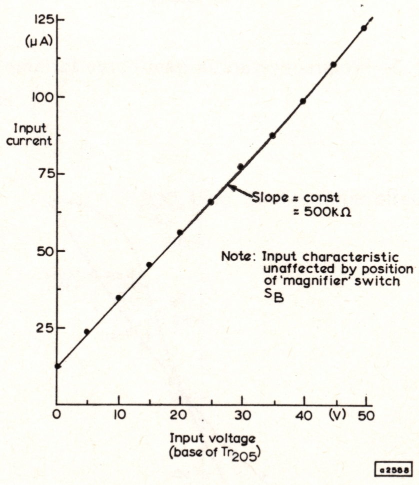


Fig. 6—Input characteristic with emitter-follower

Step cancellation is demonstrated in waveforms 5e and 6e which show the start of the 1ms ramp at 0·5V/cm and 10μs/cm and in 5f and 6f which show the start of the 2μs ramp at 0·5/cm and 40ns/cm. Linearity tests were made using the horizontal amplifier of a 545 oscilloscope, and trace blanking was achieved by means of the gating pulse from the ramp generator. These tests proved very satisfactory, and non-linearity was insignificant. The scope amplifier had insufficient bandwidth to test the 2μs sweep in the same way, so a simple differentiating circuit was used to measure the linearity of the 2μs and 1μs (with 'X2' expansion) sweeps; the constancy of slope can be estimated from the flat tops of the last waveform of Fig. 9.

TRIGGER CIRCUIT

The trigger circuit (Fig. 8) is a straightforward Schmitt trigger preceded by a buffer stage which serves to isolate the input from the trigger circuit and reduce trigger feedout to negligible proportions, and also to provide a constant input impedance of 50 to 100kΩ and 15 pF.

The trigger level control operates over a range of ±5V referred to the input, but inputs considerably greater than this can be tolerated without damage occurring. The minimum trigger voltage required at low (<1Mc/s) frequencies is 200mV pk-to-pk.

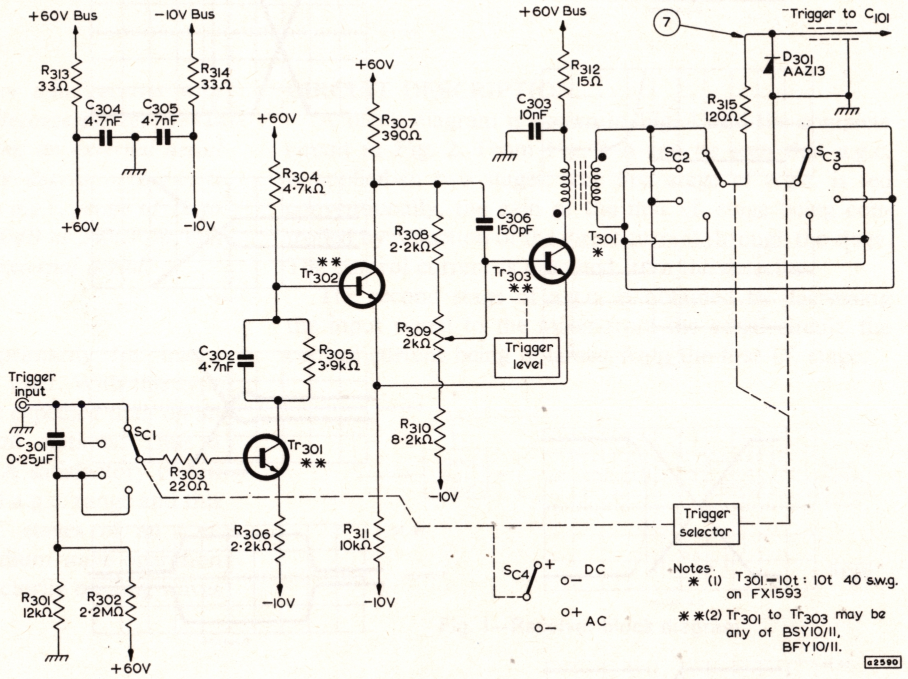

+60V Bus
−10V Bus
R313
33Ω
R314
33Ω
C304
4·7nF
C305
4·7nF
+60V
−10V
+60V
R304
4·7kΩ
+60V
R307
390Ω
+60V Bus
R312
15Ω
C303
10nF
7
Trigger to C101
D301
AAZ13
R315
120Ω
SC2
SC3
C306
150pF
R308
2·2kΩ
T301
✱
Tr302
✱✱
Tr303
✱✱
R309
2kΩ
Trigger
level
C302
4·7nF
R305
3·9kΩ
Trigger
input
SC1
C301
0·25μF
Tr301
✱✱
R303
220Ω
R310
8·2kΩ
−10V
Trigger
selector
R306
2·2kΩ
R311
10kΩ
−10V
−10V
SC4
+
−
DC
+
−
AC
R301
12kΩ
R302
2·2MΩ
+60V
Notes
✱ (1) T301 = 10t : 10t 40 s.w.g. on FX1593
✱✱(2) Tr301 to Tr303 may be any of BSY10/11, BFY10/11.
a2590

Fig. 8—Circuit of trigger stage

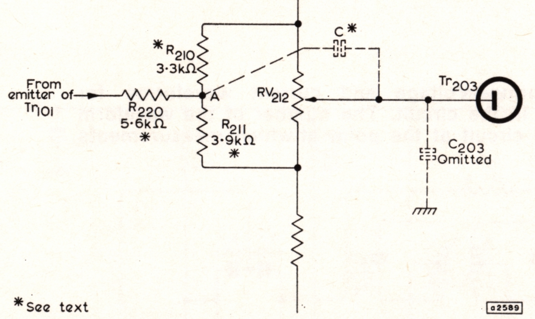

✱R210
3·3kΩ
From
emitter of
Tr101
R220
5·6kΩ
✱
A
R211
3·9kΩ
✱
RV212
C✱
Tr203
C203
Omitted
✱See text
a2589

Fig. 7—Modification to cancel step at start of ramp

The circuit is effective as a controllable slicer up to about 3Mc/s, but a useful output is available for synchronisation purposes up to 20Mc/s. The trigger output at 200kc/s is shown in waveform 7, Fig. 9, and is of 3·5V amplitude.

COMPLETE TIMEBASE PERFORMANCE

The overall performance of the circuits described is given below.

Sweep duration:	2μs to 500ms in 1:2:5 sequence, with continuously variable interpolation up to 2·5 times indicated value.
Output voltage:	100V pk-to-pk from symmetrical amplifier. 'X2' expansion facility, extending sweep range to 1μs.
Shift:	>±50V
Output loading permissible:	<15pF, <50kΩ
Trigger requirements:	>200mV pk-to-pk; max. freq. 10Mc/s
Trigger level control:	±5V up to 3Mc/s
Trigger modes:	a.c. or d.c., positive or negative edges.
Power requirements:	Approx. 50mA at +60V, 40mA at −10V.

REFERENCE

Gilbert, B., 'Emitter-timed Monostable Circuit', **Mullard Technical Communications**, Vol. 5, No. 49, July, 1961, pp. 345 to 354.

WAVEFORMS ARE SHOWN ON PAGE 282

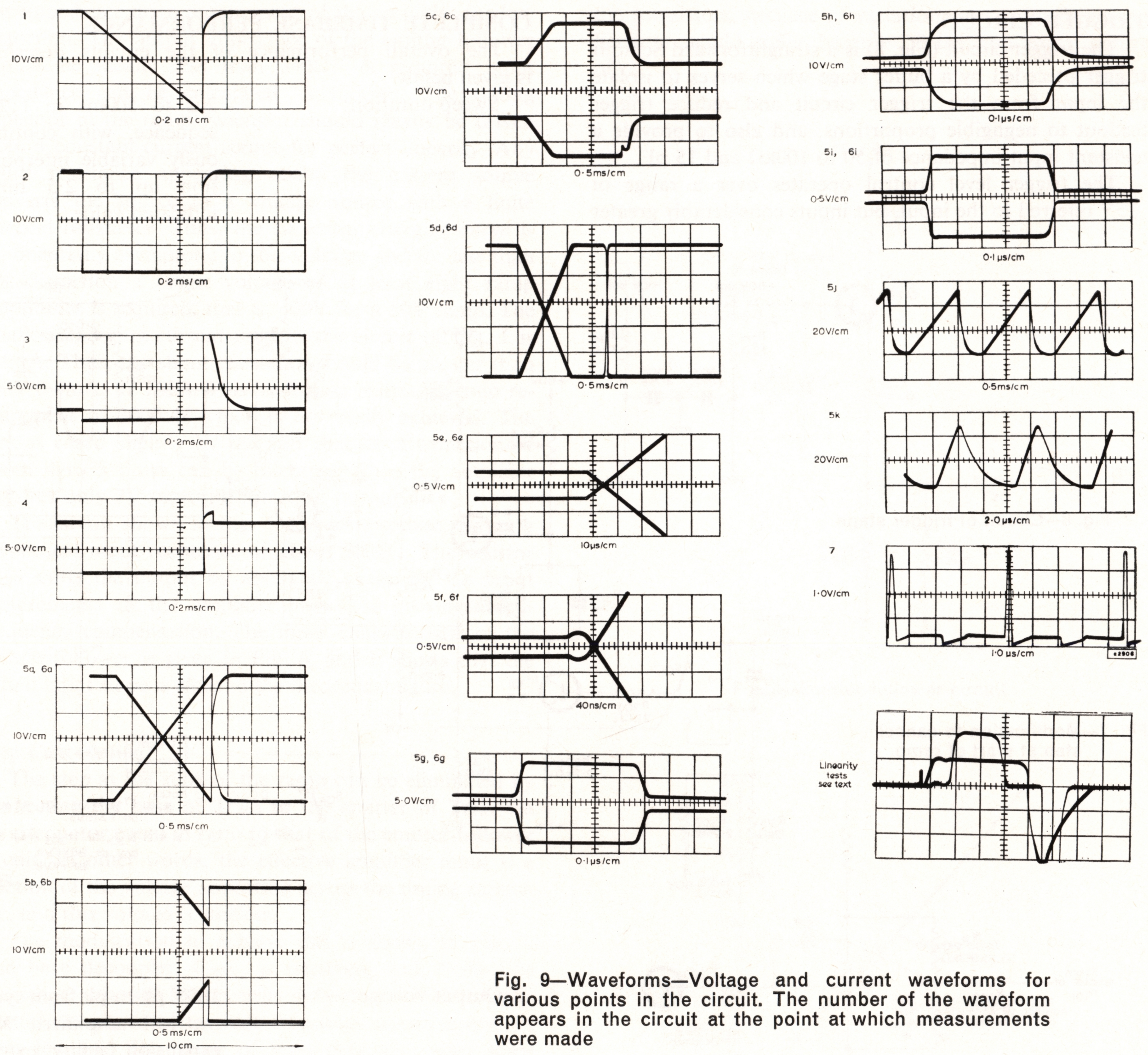


Fig. 9—Waveforms—Voltage and current waveforms for various points in the circuit. The number of the waveform appears in the circuit at the point at which measurements were made

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R.F. and I.F. Stages of a Transistor A.M. Receiver with Extended A.G.C. Range

R. E. Brown
Mullard Applications Research Laboratory

The r.f. and i.f. stages of a transistor a.m. receiver with extended a.g.c. range are described. Because the receiver is primarily intended for mains operation, an external aerial is likely to be used. Thus a greater degree of a.g.c. is required. The circuit described has an a.g.c. range of 76 to 80dB with a signal-to-noise ratio of 20dB at 240µV/m, and provides satisfactory results with an external aerial.

INTRODUCTION

When a receiver is designed primarily for mains operation, an external aerial is often used. With this type of aerial, a larger signal input can be expected than on an internal aerial, particularly on local stations. Thus a greater degree of a.g.c. is required. A satisfactory circuit has been designed giving an extended a.g.c. range and this is incorporated in the r.f. and i.f. stages of an a.m. receiver. The design given is for medium wave operation only, but the circuit functions satisfactorily on long waves as well.

CIRCUIT DESCRIPTION

A block diagram is shown in Fig. 1 and the complete circuit in Fig. 2. From Fig. 1 it can be seen that a.g.c. is applied in two stages. The first stage of a.g.c. is fed conventionally, the gain of the first i.f. stage being controlled by reduction of the direct current through the stage. The control current is obtained from the detector.

The second stage of a.g.c. is obtained by decreasing the input signal to the mixer from the aerial circuit, the control current being obtained from the first i.f. stage.

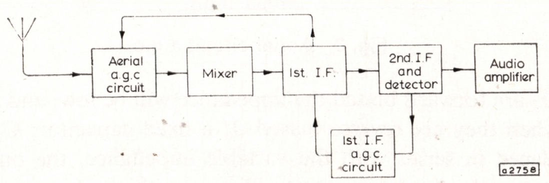
Aerial a.g.c circuit
Mixer
Ist I.F.
2nd I.F and detector
Audio amplifier
Ist I.F a.g.c circuit
a2758

Fig. 1—Receiver block diagram

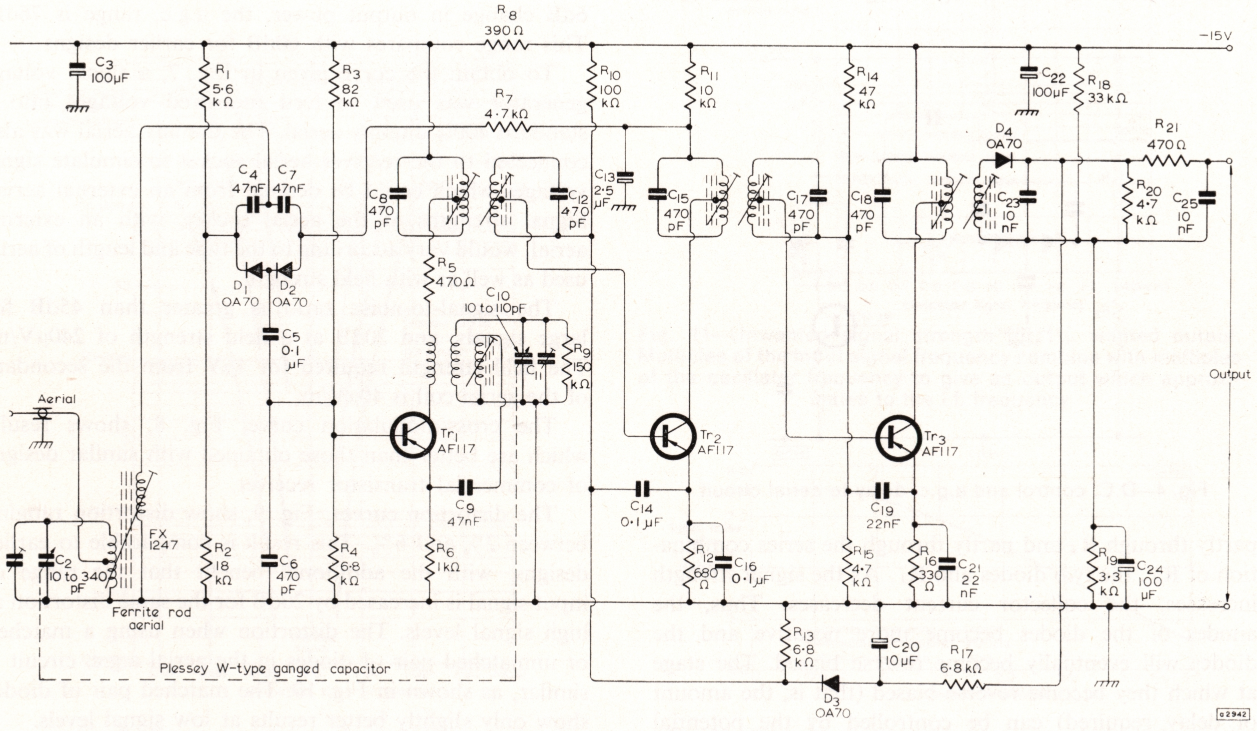
-15V
R8 390Ω
C3 100µF
R1 5·6 kΩ
R3 82 kΩ
R7 4·7 kΩ
R10 100 kΩ
R11 10 kΩ
R14 47 kΩ
C22 100µF
R18 33 kΩ
R21 470Ω
D4 OA70
C4 47nF
C7 47nF
C8 470 pF
C12 470 pF
C13 2·5 µF
C15 470 pF
C17 470 pF
C18 470 pF
C23 10 nF
R20 4·7 kΩ
C25 10 nF
D1 OA70
D2 OA70
R5 470Ω
C10 10 to 110pF
C11
R9 150 kΩ
C5 0·1 µF
Output
Aerial
Tr1 AF117
Tr2 AF117
Tr3 AF117
C9 47nF
C14 0·1 µF
C19 22nF
C1
C2 10 to 340 pF
FX 1247
R2 18 kΩ
C6 470 pF
R4 6·8 kΩ
R6 1kΩ
R12 680 Ω
C16 0·1µF
R15 4·7 kΩ
R16 330 Ω
C21 22 nF
R19 3·3 kΩ
C24 100 µF
Ferrite rod aerial
R13 6·8 kΩ
C20 10µF
R17 6·8kΩ
D3 OA70
Plessey W-type ganged capacitor
a2942

Fig. 2—Circuit diagram

Each a.g.c. current can be delayed independently to vary both the range of a.g.c. and the output available to the audio stages of the receiver.

Aerial A.G.C. Circuit

The aerial a.g.c. system is shown in Fig. 3. If it is assumed that the diodes D_1 and D_2 are forward biased, capacitor C_1 is in series with the parallel combination of C_2 and C_3. If the diodes are reverse biased, C_1 is isolated from C_2 and C_3 by the high impedance of the reverse-biased diodes. Therefore, the impedance of C_1 in series with the parallel combination of C_2 and C_3 will depend upon the bias conditions of D_1 and D_2. When D_1 and D_2 are forward biased the impedance will be low, and high when they are reverse biased. If a fixed capacitor, C_4, is placed in series with the variable impedance, the output across the fixed capacitor will vary with the bias applied to the diodes.

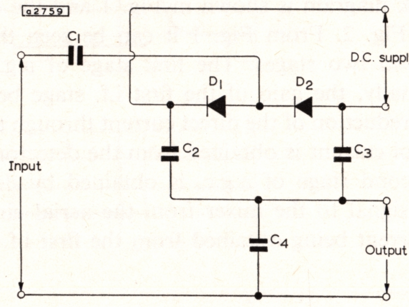

Fig. 3—Aerial circuit a.g.c.

In the receiver this variable potential divider is placed between the aerial and mixer stages (Fig. 1). The diode bias control is obtained from the first i.f. stage as shown in Fig. 4. The collector current flowing through the transistor flows partly through R_4 and partly through the series combination of R_3, the two diodes and R_1. As the signal strength increases, the collector current decreases. Thus, the anodes of the diodes become more negative and the diodes will eventually become reverse biased. The stage at which they become reverse biased (that is, the amount of delay required) can be controlled by the potential divider consisting of R_1 and R_2.

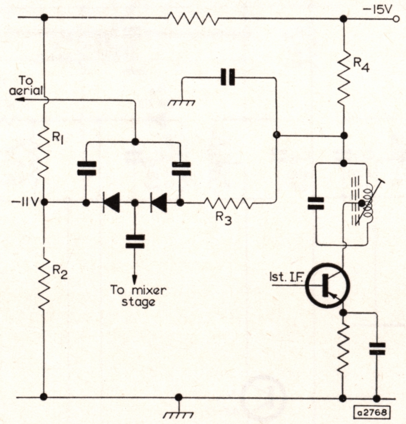

Fig. 4—D.C. control and a.g.c. delay to aerial circuit

First I.F. A.G.C. Circuit

The detector and first i.f. a.g.c. system is shown in Fig. 5. In this circuit there is a delay before the a.g.c. system comes into operation. The delay is controlled by the bias chain consisting of resistors R_1 and R_2. This bias holds the diode D_1 in reverse bias and the a.g.c. system will not operate until the output signal has reached a value which will forward-bias the diode.

So as not to load the detector circuit unduly, R_3 is placed in series with the diode. Resistor R_4 is part of the d.c. bias chain to the first i.f. transistor. Capacitor C_1 removes any audio signal that would be fed back to the first i.f. stage.

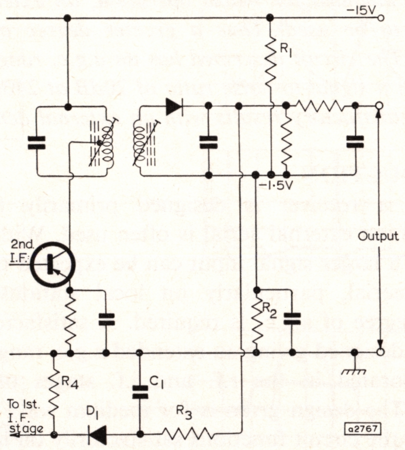

Fig. 5—A.G.C. delay to first i.f. circuit

PERFORMANCE

A.G.C. is applied over 80dB (Figs. 6 and 7). For a 6dB change in output power, the a.g.c. range is 76dB. This range compares with 60dB for earlier designs.

To obtain the curve given in Fig. 7, a signal voltage generator was used to feed measured voltages into a standard 400Ω dummy aerial. The dummy aerial was also connected to the receiver aerial socket to simulate signal voltages which could be derived from an external aerial. Signal strengths at the aerial socket, with an external aerial, would vary according to the type and length of aerial used as well as with field strength.

The signal-to-noise ratio is greater than 45dB for large signals, and 20dB at a field strength of 240μV/m. The field strength required for 1μV from the secondary of the aerial coil is 40μV/m.

The cross-modulation curve, Fig. 8, shows results which are better than those obtained with similar designs of commercial transistor receiver.

The distortion curves, Fig. 9, show distortion ranging between 2% and 6%. This result is comparable to earlier designs, with the additional benefit that the range of input signal is increased by 20dB for the same distortion at high signal levels. The distortion when using a matched or unmatched pair of diodes in the aerial a.g.c. circuit is similar, as shown in Fig. 10. The matched pair of diodes show only slightly better results at low signal levels.

Harmonic-mixing responses, Fig. 11, were obtained at

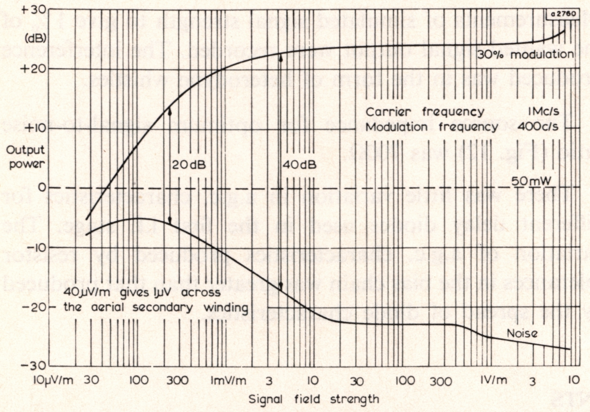

Fig. 6—A.G.C. and signal-to-noise ratio characteristics using ferrite rod aerial

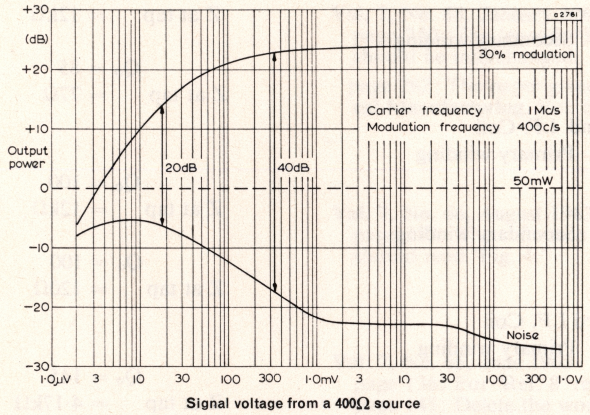

Fig. 7—A.G.C. and signal-to-noise ratio characteristics using external aerial

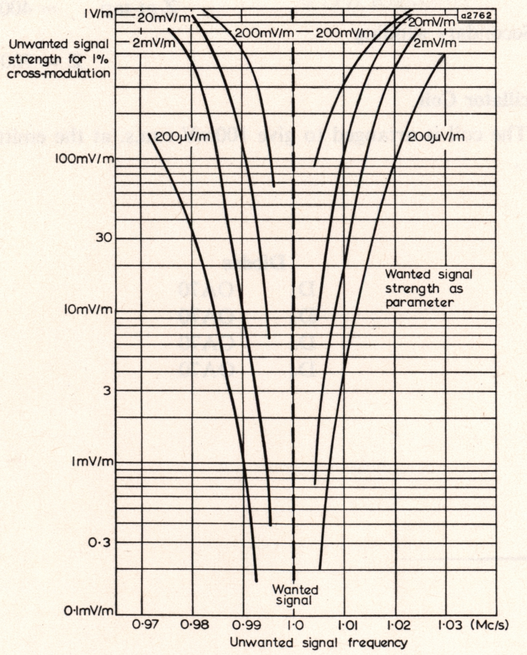

Fig. 8—Cross-modulation characteristic

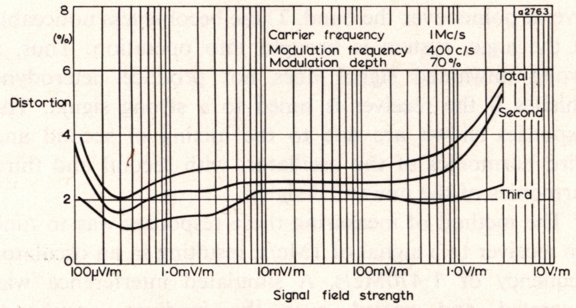

Fig. 9—Harmonic distortion versus input field strength

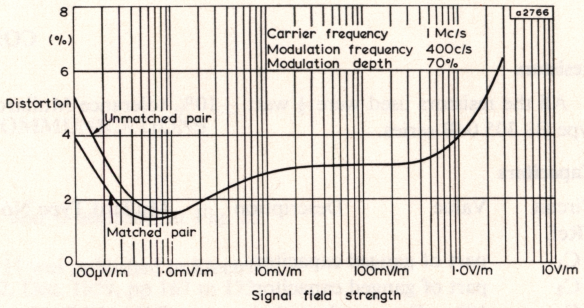

Fig. 10—Total second and third harmonic distortion versus input signal

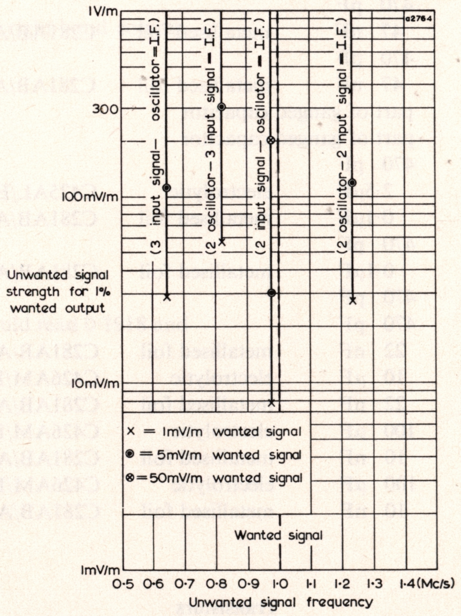

Fig. 11—Unwanted signal strength for 1% wanted output. Multiples of the input signal frequency combine with multiples of the oscillator frequency to give an output which approximates to the i.f. frequency

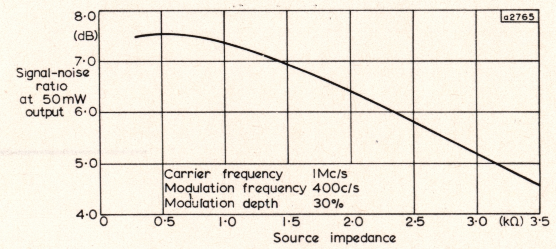

Fig. 12—Signal-to-noise ratio versus source impedance

several points over the band. These become less noticeable as the a.g.c. system is brought into operation. Thus, a strong unwanted signal does not produce heterodyne whistles if the receiver is tuned to a strong signal. The responses shown are due to the mixing of second and third harmonics of the oscillator, with second and third harmonics of the unwanted signal.

The method of measuring these responses was to tune the receiver to a signal of 1Mc/s, resulting in an oscillator frequency of 1·470Mc/s. A simulated interference was generated and varied over the medium waveband. Measurements of simulated signal strength to give 1% of the wanted signal output were recorded. The interference produced was in the form of heterodyne whistles.

The source impedance for optimum signal-to-noise ratio (Fig. 12) was 700Ω.

There was little variation in a.g.c. characteristics for different delay diodes used in the first i.f. stage. The variation of a.g.c. characteristics produced by resistor tolerances in the bias chain was greater than that produced by the spread of diode characteristics.

COMPONENTS

Resistors

All the resistors used were $\frac{1}{8}$ watt ±10% tolerance Mullard type B8 305 04B series.

Capacitors

Circuit Ref.	Value	Description	Mullard Type No.
C_1	part of ganged capacitor		
C_2	part of ganged capacitor		
C_3	100 µF	electrolytic	C426AM/E100
C_4	47 nF	metallised foil	C281AB/A47K
C_5	0·1µF	metallised foil	C281AB/A100K
C_6	470 pF		
C_7	47 nF	metallised foil	C281AB/A47K
C_8	470 pF		
C_9	47 nF	metallised foil	C281AB/A47K
C_{10}	part of ganged capacitor		
C_{11}	part of ganged capacitor		
C_{12}	470 pF		
C_{13}	2·5µF	electrolytic	C425AL/E2·5
C_{14}	0·1µF	metallised foil	C281AB/A100K
C_{15}	470 pF		
C_{16}	0·1µF	metallised foil	C281AB/A100K
C_{17}	470 pF		
C_{18}	470 pF		
C_{19}	22 nF	metallised foil	C281AB/A22K
C_{20}	10 µF	electrolytic	C426AM/E10
C_{21}	22 nF	metallised foil	C281AB/A22K
C_{22}	100 µF	electrolytic	C426AM/E100
C_{23}	10 nF	metallised foil	C281AB/A10K
C_{24}	100 µF	electrolytic	C426AM/B100
C_{25}	10 nF	metallised foil	C281AB/A10K

Transistors

Tr_1	AF117
Tr_2	AF117
Tr_3	AF117

Coil Data

1st I.F. Coil

Primary winding

$Q_o = 85$

Z at tap = 12kΩ

Secondary winding

$Q_o = 85$

Z at tap = 77Ω

2nd I.F. Coil

Primary winding

$Q_o = 100$

Z at tap = 12kΩ

Secondary winding

$Q_o = 100$

Z at tap = 120Ω

3rd I.F. Coil

Primary winding

$Q_o = 145$

Z at tap = 4·17kΩ

Secondary winding

Tap-to-secondary ratio = 1·58:1

Aerial Coil

Primary winding

$Q_o = 150$

Z at tap = 400Ω

Secondary winding

Z = 700 Ω

Oscillator Coil

The coil is arranged to give 100mV r.m.s. at the emitter of Tr_1.

Diodes

D_1	OA70
D_2	OA70
D_3	OA70
D_4	OA70

MULLARD TECHNICAL COMMUNICATIONS

Vol. 7, No. 68, January 1964

page 250: The legends '1 section' and '3 sections' in Fig. 25 should be interchanged.

page 262: The paper given as Ref. 11 was published in **Electrical Manufacturing,** Vol. 64, No. 12, Dec. 1959, pp 167 to 173.

Vol. 7, No. 66, August 1963

page 173: The reference to Fig. 3 in the right-hand column should read 'Fig. 4.'

Vol. 7, No. 65, June 1963

page 136: For 'Ref. 8' read 'Ref. 10'.

page 145: Delete the words 'Ref. 4'.

Vol. 7, No. 64, May 1963

page 105: The values 191·8 and 196·1 should read 0·1918 and 0·1961 respectively.